REMARKS

The Office Action dated January 16, 2008 indicated an objection to the drawings as well as the following claim rejections: claims 1-10 stand rejected under 35 U.S.C.§102(b) over the Kuroda reference (U.S. Patent Pub. 2001/0039643) and claims 1-10 stand rejected under 35 U.S.C. § 103(a) over the Hsu reference (U.S. Patent No. 7,272,803) in view of one or more of the Vitek reference (U.S. Patent No. 7,047,515) and the Culler reference (U.S. Patent No. 6,370,678).

Applicant believes the amendments to the drawings should overcome the objections thereto.

Applicant respectfully traverses the Section 102 rejection over the '643 (Kuroda) reference because the rejection relies solely upon figures 3, 4 and 6, none of which provides correspondence to all of the claim limitations as suggested in the Office Action. Essentially, these figures show non-logic cells having a pair of transistors connected between power supplies, which fail to disclose the claimed decoupling cells and constant circuit distance, and fail to recognize any problem relating to the same. For example, referring to claim 1, an integrated circuit has a power distribution network that supplies power from respective power and ground pads to a plurality of circuit elements on the integrated circuit. The decoupling cells between the power and ground pads maintain, for any given circuit element on the integrated circuit, a "combined distance between the power pad and said circuit element, and between the ground pad and said circuit element."

Cited figures 3, 4 and 6 in the '643 reference do not disclose the claimed decoupling cells, the claimed power distribution network, or maintaining any combined distance between a circuit element and respective power and ground pads as relevant to claim 1 as discussed above, and to claims 2-10 that depend therefrom. FIG. 3 shows non-logic cells having two transistors for arrangement in connection with a circuit design approach. FIG. 4 and FIG. 6 also show non-logic cells, each cell having a p-type MOS transistor and an n-type MOS transistor that are respectively coupled between power supply lines VDD and VSS. FIG. 6(B) shows an equivalent circuit, where these transistors are coupled in parallel between VSS and VDD, with no apparent connection to any circuit element. None of these non-logic cells are shown connected to any circuit element as claimed, and do not form a power distribution network that maintains any distance between respective power and

ground pads and such a circuit element. The Office Action has cited no supporting discussion and provided no explanation as to how these transistors relate to the claim limitations, or to where in these cited figures the alleged correspondence lies.

In addition to the above, the non-logic cells in figures 3, 4 and 6 also fail to disclose limitations in various dependent claims, such as those in claim 2 directed to increasing and decreasing respective circuit distances between a circuit element and both power and ground pads to maintain an overall distance that is constant. As shown in the equivalent circuit of FIG. 6(B) and applicable to each of figures 3, 4 and 6, the respective transistors are fixed with what appears to be a consistent distance between VDD and VSS. Therefore, there appears to be no manner in which to maintain a consistent combined distance (*e.g.*, increase one distance and decrease a different distance) between respective pads and a circuit element.

In view of the above discussion, the cited portions of the '643 reference (figures 3, 4 and 6) do not provide correspondence to all of the claimed limitations. Accordingly, the Section 102 rejections are improper and should be removed.

Applicant respectfully traverses the Section 103 rejections because the cited references fail to provide correspondence to all of the claim limitations, and further because there is no motivation to combine the cited references as proposed in the Office Action. As relative to claim 1 and the above discussion thereof, the '803 (Hsu) reference does not teach or suggest claim limitations directed to any circuit that maintains a constant distance between a circuit element and respective power and ground pads. Specifically, cited figures 2-5 and corresponding column 6 describe power grid structures having parallel stripes having a physical grid arrangement that may be "evenly spaced." The physical grid arrangement is used to make a power grid structure having a reduced number of vias "to be especially beneficial to 45° or 135° diagonal wiring paths" as described in the Abstract of the '803 reference. These cited portions make no mention of how these parallel power grid stripes are connected to any circuit elements to maintain a constant combined distance as claimed or otherwise. It appears that the Office Action is misinterpreting this "even" physical grid spacing as a "constant" combined circuit distance (length) between a circuit element and respective power and ground pads. Applicant submits that this even physical spacing is unrelated to any circuit length, to the claimed power distribution network and its

function of maintaining combined circuit distances constant. Accordingly, the cited portions of the primary '803 reference also fail to teach or suggest limitations in other claims, such as those in claim 2 as directed to increasing and decreasing respective circuit element-to-pad distances for both power and ground pads.

In addition to the above, the asserted motivation for combining the references as proposed is insufficient to establish or maintain a Section 103 rejection because there is no evidence as to why one of skill in the art would be motivated to make the proposed combination. Specifically, the motivation alleged at page 4 of the Office Action states that "[d]ecoupling/bypass cells/capacitors are well known in the art" and that they are "conventional for controlling transient noise." As is consistent with relevant law (*e.g.*, based on the recent U.S. Supreme Court decision as to teaching/suggestion/motivation under §103), for a rejection to be maintained under §103, the rejection must present some proper reason why a skilled artisan would change the main reference as proposed. *See KSR Int'l Co. v. Teleflex Inc.*, 127 S. Ct. 1727, 1741 (U.S. 2007) ("A patent composed of several elements is not proved obvious merely by demonstrating that each element was, independently, known in the prior art.") In this regard, the citation to decoupling/bypass components asserted as well-known or conventional and independently known are insufficient to support their combination with the primary '803 reference. In this regard, there is no motivation for modifying the primary '803 reference and the rejection should be reversed.

New claims 11 - 17 are also allowable over the cited references for the reasons stated above, as relevant to claim limitations that are directed to subject matter including a power distribution circuit that is not disclosed, taught or suggested in any of the cited references. Moreover, the cited references do not disclose, teach or suggest limitations directed to decoupling cells that selectively decouple circuits between a circuit element and either/or a power pad and a ground pad. Support for these claims may be found, for example, at paragraph 0020.

In view of the above, Applicant believes that each of the rejections/objections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Peter Zawilski, of NXP Corporation at (408) 474-9063.

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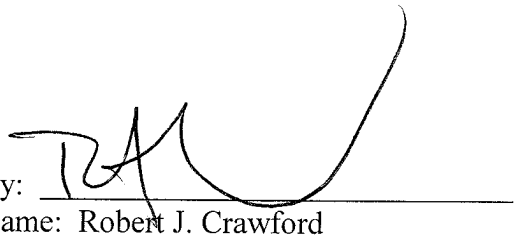
By: 
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